REMARKS/ARGUMENTS

Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-49 of copending Application No 11/246,309.

The applicant respectfully disagrees with the Examiner's analysis of the difference between claim 1 of the present invention and copending application No 11/246,309. In the Office action of 03/19/2008, the Examiner presented a table comparing claim 1 of the present invention with claim 1 of copending application 11/246,309. However, the table presented by the Examiner does not take into account any of the amendments already made to further define the scope of the present invention claimed by independent claim 1, or the amendments already made to further define the scope of claim 1 of the copending application No 11/246,309.

The correct table comparing the differences (shown in bold) of claim 1 of the present invention and claim 1 of copending application 11/246,309 is shown below:

Present invention	**Application 11/246,309**
A storage virtualization computer system comprising: a host entity for issuing IO requests; an external storage virtualization controller coupled to said host entity for executing IO operations in response to said IO requests; and at least one physical storage device (PSD), each coupled to the storage virtualization controller through a **point-to-point serial-signal** interconnect, for providing storage to the storage virtualization computer system through the storage virtualization controller; wherein said storage virtualization controller comprises:	A storage virtualization computer system comprising: a host entity for issuing IO requests; an external storage virtualization controller coupled to said host entity for executing IO operations in response to said IO requests; and at least one physical storage device (PSD), each coupled to the storage virtualization controller through **a SAS interconnect**, for providing **data** storage space to the storage virtualization computer system through the storage virtualization controller; wherein said external storage virtualization controller comprises:

a central processing circuitry for performing **said** IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to said host entity; and at least one **device-side IO** device interconnect port provided in one of said at least one IO device interconnect controller for coupling to one of said at least one physical storage device **through said point-to-point serial-signal interconnect, said device-side IO device interconnect port being a serial port for point-to-point serial-signal transmission;** **wherein said computer system further comprises a detachable canister attached to said storage virtualization controller for containing one of said at least one PSD therein;** wherein said storage virtualization controller is configured to define at least one logical media unit consisting of sections of at least one said PSD; **and** **wherein said SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying IO data into at least one data packet for transmission to said**	a central processing circuitry **(CPC)** for performing IO operations in response to said IO requests of said host entity; at least one IO device interconnect controller coupled to said central processing circuitry; at least one host-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to said host entity; and at least one **SAS** device-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to one of said at least one physical storage device; and wherein said storage virtualization controller is configured to define at least one logical media unit consisting of sections of at least one said PSD..

PSD through said device-side IO device interconnect port.	

Because all the independent claims of the present invention have been amended in a similar manner, the bolded claim limitations shown above are also included in the other claims of the present invention through their respective dependencies.

As should be apparent to the Examiner upon inspection of the above table, it is not true that "Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application", as was stated by the Examiner in the Office action of 03/19/2008. In particular, there are detailed and patentably distinct claim features in the present invention, see the bolded differences shown in the above table, that are not disclosed in or claimed by the copending application. For this reason, these claimed features would also not be covered by any patent that might be issued on copending application 11/246,309.

In view of these arguments, the applicant respectfully requests that the Examiner withdraw the provisional double patenting rejection with respect to copending application 11/246,309.

Claims 1-16, 20-37, 41-46, 50, 78-83, 86-88, 90-94, and 96 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218).

(1) Improper rejections of independent claims 1, 21, 78, and 90 - applicant requests correction

The applicant firstly points out that the Examiner's rejection of the independent claims 1, 21, 78, and 90 in the Office action of 03/19/2008 is improper because it is directed at claims not found in the present invention and therefore should be withdrawn. Specifically, the Examiner appears to have confused the independent claims of the present invention with another case.

The problems start on page 7 of the Office action of 03/19/2008 where, concerning the teachings of Bicknell, the Examiner writes "but fails to disclose

expressly 'transmission with SAS protocol and wherein the redundant SVC pair ...." The applicant notes that the features stated in this section by the Examiner as not being taught by Bicknell are not claimed by the present invention.

The Examiner then continued on page 7 stating, "Meehan discloses transmission with SAS protocol (**see para. 0029**) and wherein the redundant SVC pair..." This continues onto page 8 with the Examiner pointing out where Meehan discloses "SAS device-side IO deice interconnect port", and "SAS transmission" several times. However, the applicant again notes that neither claim 1 nor any other claim of the present invention claim "SAS protocol", "SAS device-side IO deice interconnect port", "SAS transmission", or "a redundant SVC pair".

For the record, the applicant has located at least the follow mistakes in the Office action of 03/19/2008:

(a) "SAS protocol and wherein in the redundant SVC pair" on page 7, lines 1 to 2.

(b) "SAS device-side IO device interconnect port" on page 7, lines 7.

(c) "transmission with SAS protocol" on page 7, line 15.

(d) "SAS device-side IO device interconnect port" on page 8, lines 5.

The applicant notes that MPEP 707.07 states that the Examiner's action should be both complete and clear. The applicant asserts that because the claim features argued by the Examiner in the Final office action of 03/19/2008 are not found in the present invention, the rejections of the independent claims 1, 21, 78, and 90 are not clear. In other words, it is not fair to the applicant because the applicant is not clear on how the current independent claims 1, 21, 78, and 90 are actually being rejected. Therefore, the applicant cannot appropriately include arguments to show how the rejections are overcome until the rejections are stated in a proper way.

The applicant also points out that MPEP section 710.06 states that when "an Office action contains some other error that affects applicant's ability to reply to the Office action and this error is called to the attention of the Office ... If the error is brought to the attention of the Office within the period for reply set in the Office action but more than 1 month after the date of the Office action, the Office will set a new period for reply, if requested to do so by the applicant, to substantially equal the

time remaining in the reply period." The applicant notes that the same MPEP section also states, "The new period for reply must be at least 1 month and would run from the date the error is corrected."

The applicant hereby officially calls to the attention of the Examiner that there errors in the rejection of the independent claims 1, 21, 78, and 90 that affect the applicant's ability to reply to the Office action and requests that the rejections are fixed to properly refer to the independent claims of the present invention so that applicant can appropriately reply.

(2) Comments regarding patentability claims 1, 21, 78, and 90

(2a) The Examiner deemed that "wherein said SVC issues a device-side IO request to said IO device interconnect controller, and IO device interconnect controller **re-formats** said device-side IO request and accompanying IO data into **at least one data packet** for transmission to said PSD through said device-side IO device interconnect port. (see para.0029, which discloses the FPGA 409 "manipulating" data between the host and the storage devices. Manipulating is a form of "re-formatting". The claim language is not specific as to how this reformatting is being done. See also para.0016, which discloses "re-distributed" the data" on page 8, lines 14 to 20 in the OA. However, applicant respectfully argues and explains as follows:

(a) "The claim language is not specific as to how this reformatting is being done" asserted by examiner is claimed in claims 89 and 95 of the present invention, take claim 89 for example, "wherein said **data packet** comprises **a start segment** at the beginning indicating the start of said data packet, **an end segment** at the end indicating the end of the data packet, **a payload data segment** containing actual IO information to transmit through the device-side IO device interconnect, and **a check data segment** containing check codes derived from said payload data for checking the correctness of said payload data after transmission."; in other words, claim 89 and 95 of the present invention have defined how this reformatting is being done", i.e., according to the independent claims of the present invention, the present invention **re-formats** said device-side IO request and accompanying IO data into **at least one data packet,** in which **the**

data packet comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission (please refer to Fig.10 and para.0071 and 0072).

In contrast, point 41 in the OA, paragraph 0025 of Johnson only discloses "several parameters, such as **Initial Strip Size for indicating the size (i.e., the number of bytes) of the initial block of data** (e.g., metadata or header information) to be transferred for the first stripe of the drive, **an Initial Skip Size for indicating an amount of the drive** (i.e., the number of bytes) to skip prior to transferring data for the drive, **a Stripe Size for indicating the size** (i.e., the number of bytes) in a single stripe, and **a Stripe Skip for indicating the amount of the drive to skip** after transferring a stripe of data. Alternatively, parameter information may included **a set of absolute addresses,** each having **a start address and an end address, that determine the data that is to be transferred from host memory to the disk drives or determine where data is to be stored when transferred from the disk drives to host memory".** From the aforesaid paragraph, it can be concluded that para.0025 of Johnson only discloses as follows:

(a1) **Initial Strip Size** for indicating the size (i.e., the number of bytes) of the initial block of data;

(a2) **an Initial Skip Size** for indicating an amount of the drive (i.e., the number of bytes) to skip prior to transferring data for the drive;

(a3) **a Stripe Size** for indicating the size (i.e., the number of bytes) in a single strip;

(a4) **a Stripe Skip** for indicating the amount of the drive to skip; and

(a5) **a set of absolute addresses,** each having **a start address and an end address**, that determine the data that is to be transferred from host memory to the disk drives or determine where data is to be stored when transferred from the disk drives to host memory.

Please be noted that, in the claimed invention, "**the start segment**" is a segment in a data packet indicating the beginning of the data packet, which tells the receiving device that a new data packet is now being transmitted to and will be received by the receiving device, while "**a start address**" disclosed in the Johnson tells the receiving device where in the memory it can access the data, and if the receiving device of such information has the function of performing data accessing, it can access the data in the memory according to the start address. Therefore, "**the start segment**" in the claimed invention and "**a start address**" disclosed in the Johnson are totally different things. Similarly, in the claimed invention, "**the end segment**" is a segment in a data packet indicating the end of the data packet, which tells the receiving device that the data packet has being transmitted to completion and the will be no more data belonging to that data packet being transmitted to the receiving device, while "**an end address**" disclosed in the Johnson tells the receiving device where in the memory the last data to be transferred exists, and if the receiving device of such information has the function of performing data accessing, it can access the last data in the memory according to the end address. Therefore, "**the end segment**" in the claimed invention and "**an end address**" disclosed in the Johnson are totally different things.

In conclusion, para. 0025 of Johnson disclosed something totally different from the claimed invention. Therefore, para.0025 of Johnson **fails to teach or suggest** "**re-formatting** said device-side IO request and accompanying IO data into **at least one data packet** for transmission to said PSD through said device-side IO device interconnect port, in which **the data packet** comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission" in claims 89 and 95 of the present invention.

(2b) Para.0029, lines 15 to 20 of Meehan only discloses "Given that the RAM 407, ROM408, and FPGA 409 are **manipulating** the data to and from the storage

devices, it would be possible to manage the data in any desired form required by/ for the storage devices", **but fails to teach or suggest** "**re-formatting** said device-side IO request and accompanying IO data into **at least one data packet** for transmission to said PSD through said device-side IO device interconnect port in independent claims of the present invention, in which **the data packet** comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission" in claims 89 and 95 of the present invention.

(2c) Para.0016 of Meehan only discloses "this RAID architecture can implement a RAID 4/5 at the primary RAID controller 205 and a RAID 0 at the secondary RAID controllers 210. The data received by each secondary RAID controllers 210 is then **re-distributed** to the lower level nodes"; in other words, the data received by each secondary RAID controller 210 is evenly written (striped) in a RAID 0 stripe (i.e., RAID 0 means striping which evenly divides data to be stored into several stripes, and then **evenly distributes** the several stripes to the lower level nodes (storage devices)), but para. 0016 of Meehan fails to teach or suggest "**re-formatting** said device-side IO request and accompanying IO data into **at least one data packet** for transmission to said PSD through said device-side IO device interconnect port in independent claims of the present invention, in which **the data packet** comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission" in claims 89 and 95 of the present invention.

Further comments regarding the patentability of particular dependent claims are presented in the following paragraphs.

Comments regarding patentability claims 13 and 29

Claims 13 and 29 of the present invention claim "wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side device interconnect ports."

Moreover, please refer to paragraph [0098] of the present invention, in which another feature that an SVC might implement is redundancy in the host-side interconnects in which multiple host-side interconnect ports are included on the SVC and LMUs are presented to the host identically over two or more of these interconnects. This feature is designed to allow the host the ability to maintain access to the LMU even if one of the interconnects and/or ports on the interconnect should break, become blocked or otherwise malfunction. That is, said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side device interconnect ports twice.

In contrast to the present invention as claimed, paragraph [0019] of Bicknell only discloses "Disc drive 106 also includes a data interface 144.....due to disc drive failure", Please refer to Fig. 6 of Bicknell, in which two controllers, CONTROLLER 1 and CONTROLLER 2, are shown and each has only one interconnect coupled to a HOST COMPUTER to its left. Obviously, Bicknell does not disclose or suggest a controller having two ports connecting to a host for redundantly present a LMU the host. Therefore, Bicknell fails to teach or suggest "wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side device interconnect ports", as is claimed in claims 13 and 29 of the present invention.

Comments regarding patentability claims 34 and 96

Claims 34 and 96 of the present invention claim "wherein said storage virtualization controller further comprises at least one multiple-device device-side expansion port for accommodating an additional set of at least one PSD."

Please refer to paragraph [0092] of the present invention stating, "because the S-ATA specification only allows for maximum signal line lengths of 1.5 m, the PSDs

connected to one SVC must be packed close enough so that no signal line length exceeds 1.5m. A typical S-ATA storage virtualization subsystem will only provide for connection of a maximum of 16 S-ATA PSDs because of these limitations. So a "pure" S-ATA storage virtualization subsystem is unable to match the expandability of a Fibre FC-AL storage virtualization subsystem, which will typically allow for connection of up to 250 PSDs via connection of external expansion chassis on the same set of device-side IO device interconnects." Also please refer to paragraph [0093] of the present invention stating, "In order to overcome this limitation, the present invention optionally includes one or more expansion device-side multiple-device IO device interconnects, herein referred to as device-side expansion ports, such as Parallel SCSI or Fibre FC-AL on the SVC. These interconnects will typically be wired in such a way as to allow external connection of external expansion chassis. These chassis could be simple "native" just a bunch of drives (JBODs) of PSDs directly connected to the interconnect without any intervening conversion circuitry or could be intelligent JBOD emulation subsystems that emulate "native" JBODs using a combination of S-ATA or P-ATA PSDs and a single or redundant set of SVCs that provide the conversion from the multiple-device IO device interconnect protocol that provides the connection of the JBOD subsystem to the primary storage virtualization subsystem to the device-side IO device interconnect (S-ATA or P-ATA) protocol that provides the connection between the JBOD SVC(s) and the PSDs that they manage."

Therefore, in claims 34 and 96 of the present invention, said storage virtualization controller further comprises at least one multiple-device device-side expansion port for accommodating an additional set of at least one PSD. Moreover, please refer to figs. 3, 17 and 18, in which in fig.3, there are 16 S-ATA interconnects 201 connected to local physical storage device array (PSD) 400 which comprises a plurality of physical storage devices 420. However, please refer to figs. 17 and 18, in which in addition to the 16 Serial ATA interconnects that are connected to local PSD 400 (please refer to fig.3), storage virtualization controller (SVC) can have more expansion subsystems (i.e., an additional set of at least one PSD in claims 34 and 96) through the device-side expansion port for accommodating an additional set of at

least one PSD (i.e., expansion subsystem in figs. 17 and 18).

In contrast to the present invention, the Midplane Card ports 209 of Fig. 6 of Bicknell only discloses the midplane card ports 209 are connected to data ports 204 of controller, which does not disclose an additional set of HDDs, and thus fails to teach or suggest "wherein said storage virtualization controller further comprises at least one multiple-device device-side expansion port for accommodating an additional set of at least one PSD." Therefore, the applicant respectfully asserts that Bicknell does not teach or suggest "wherein said storage virtualization controller further comprises at least one multiple-device device-side expansion port for accommodating an additional set of at least one PSD", as is claimed in claims 34 and 96 of the present invention.

Claims 11 and 25 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US pub 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above , and further in view of Otterness et al. (US pub. 2002/0152355).

Claims 11 and 25 are dependent upon claims 1 and 21, respectively, and therefore the rejections of these claims inherit the problems described above for the independent base claims and are also asserted to be improper by the applicant.

Claims 17, 19, 38, 40, 47, 48, 84, and 85 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US pub 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above , and further in view of Rabinovitz et al. (US pat. 6,483,107).

Claims 17, 19, 38, 40, 47, 48, 84, and 85 are dependent upon claims 1 and 21, respectively, and therefore the rejections of these claims inherit the problems described above for the independent base claims and are also asserted to be improper by the applicant.

Claims 18, 39, 49, 51, 52, and 53 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US pub 2003/0193776) in view of Meehan et al.

(US pub. 2004/0177218) as applied to claim 1 above , and further in view of Colton (US pub. 2005/0089027).

Claims 18, 39, 49, 51, 52, and 53 are dependent upon claims 1 and 21, respectively and therefore the rejections of these claims inherit the problems described above for the independent base claims and are also asserted to be improper by the applicant. Further comments regarding the patentability of these claims are presented in the following paragraphs.

Comments regarding patentability claims 18 and 39

Concerning claims 18 and 39, the Examiner stated in the Office action of 03/19/2008 that "Colton discloses Ethernet supporting the iSCSI protocol operating in target mode (see fig.11 and paragraph 1487, which discloses internet SCSI in an Ethernet network)." However, the applicant respectfully disagrees. In particular, neither paragraph 1487 of Colton nor any other paragraph of Colton discloses the iSCSI protocol operating in target mode. (emphasis added). Instead, paragraph 1487 only states, "The Sum server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance", and figure 11 of Colton also does not illustrate or mention anything about target mode of iSCSI protocol. The applicant also has done a search of the full text of Colton and the word "target" does not occur anywhere in the text of Colton.

Additionally, fig. 6 of Bicknell fails to disclose host-side IO device interconnect port, and fig. 11 and paragraph 1487 of Colton only discloses 2 high-speed SCSI disk drives to ensure adequate performance, but fails to discloses iSCSI protocol operating in target mode. In addition, it should be reminded that the Colton relates to optical transport system and Dense Wave Division Multiplexing(DWDN). On the contrary, the instant application relates to storage virtualization system, both of which belong to different fields of invention.

For at least these reasons, the applicant respectfully asserts that Colton should not be relied upon to support the claimed feature "wherein at least one said hostside IO device interconnect port is Ethernet supporting the iSCSI protocol operating in target mode" (emphasis added), as is claimed in claims 18 and 39 of the present

invention.

Claims 89 and 95 are rejected under 35 USC 103a as being unpatentable over Bicknell et al. (US pub 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) as applied to claim 1 above, and further in view of Johnson et al. (US pub. 2003/0033477).

Claims 89 and 95 are dependent upon claims 1 and 21, respectively and therefore the rejections of these claims inherit the problems described above for the independent base claims and are also asserted to be improper by the applicant. Further comments regarding the patentability of these claims are presented in the following paragraphs.

Comments regarding patentability claims 89 and 95

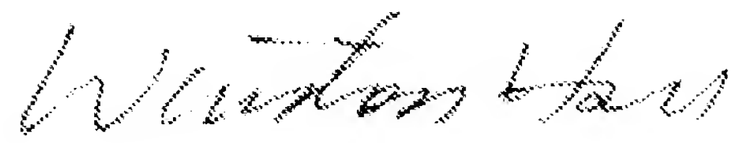
On page 8, lines 14 to 20 in the in the rejection of claim 1 in the Office action, please refer to arguments in independent claims 1, 21, 78, and 90 of this paper.

In conclusion, in view of all of cited references, claims 89 and 95 are patentably distinct from them, can thus have patentability and are allowable.

Conclusion:

The Examiner is encouraged to telephone the undersigned if there are informalities or other issues that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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